



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2841  
Examiner: Yuriy Semenenko

In Re PATENT APPLICATION of:

Applicant(s): Seiichiro SASAKI et al.

Serial No.: 10/812,962

Filing Date: March 31, 2004

For: MULTILAYERED POWER SUPPLY  
LINE FOR SEMICONDUCTOR  
INTEGRATED CIRCUIT AND LAYOUT  
METHOD THEREOF

Atty. ref.: OKI 417

**RESPONSE TO  
RESTRICTION  
REQUIREMENT**

March 9, 2006

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Responsive to the Restriction Requirement mailed on February 16, 2006, Applicants elect the invention of Group I, i.e., the subject matter of claims 1-7, for further examination. The election is made without traverse.

Examination of the application on the merits is respectfully requested.

Respectfully submitted,

March 9, 2006  
Date

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RHB/vm